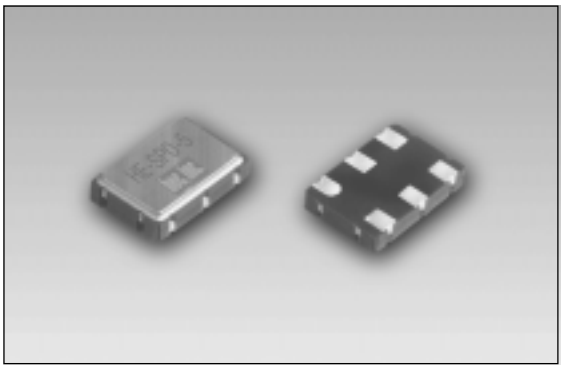
HE-SPO-5 / HE-SPO-3 PROGRAMMABLE OSCILLATOR

The HE-SPO-5 / HE-SPO-3 programmable oscillator series allows for a very wide frequency range and 5V, 3.3V, or dual voltage options. This oscillator is available in TTL, CMOS, and PECL output options, and is packaged in the compact industry standard 5x7mm ceramic SMD case.

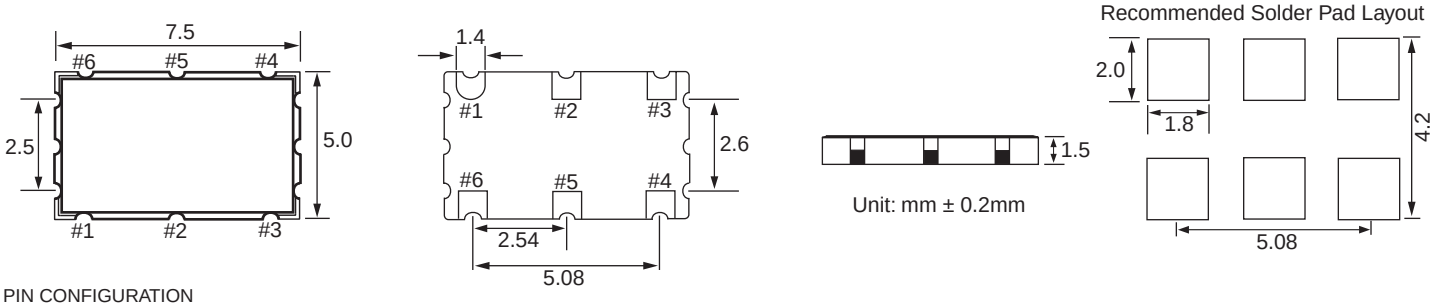


FEATURES:
- TTL, CMOS, or PECL output option
- Single 5V, 3.3V, or dual voltage option
- Wide frequency range 340 kHz up to 250 MHz
- Powerdown or Enable/Disable Options

ELECTRICAL SPECIFICATIONS

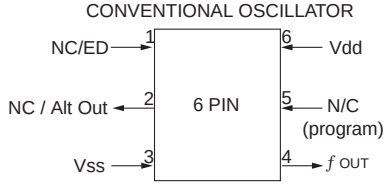
PARAMETERS		SPECIFICATIONS			
HEC PN		**HE-SPO-5**	**HE-SPO-3**	**HE-SPO-D**	**UNIT**
SUPPLY VOLTAGE		+5.0Vdc ± 10%	+3.3Vdc ± 0.3Vdc	+5.0V / 3.3V	Vdc
FREQUENCY RANGE		340 kHz - 250 MHz			
FREQUENCY STABILITY		A=±25 PPM, B=±50 PPM, C=±100 PPM, S=See Spec.			PPM
OPERATING TEMPERATURE		-10°C to +70°C Standard / -40 °C to +85°C Optional (-EXT)			
STORAGE TEMPERATURE		-55°C to +125°C			
OUTPUT SYMMETRY		40/60% or 45/55% (@ 1/2 Vdd)			
RISE AND FALL TIME		5.0ns 5.0ns	10 to 90% Vdd 90 to 10% Vdd		
INPUT CURRENT		45 mA max.	25 mA max.		mA
OUTPUT VOLTAGE	V_{OL} V_{OH}	Vdd: 0.4V Max @ I_{OH} = 40mA Vdd: -0.5V Min @ I_{OH} - -40mA			
	V_{OL} (PECL) V_{OH} (PECL)	Vdd: -2.0V Min. Vdd: -1.6V Max. Vdd: -1.0V Min. Vdd: -0.8V Max.			
OUTPUT LOAD		(Vdd = 3.3V) HCMOS ≤ 100.000 MHz 15pF HCMOS Load Max. ≥ 100.000 MHz 10pF HCMOS Load Max.			
		(Vdd = 5.0V) HCMOS < 100.000 MHz 25pF HCMOS Load Max. > 100.000 MHz 10pF HCMOS Load Max.			
OUTPUT OPTIONS		PECL OPTION (-PECL)			
Note: A 0.01µF bypass capacitor is recommended between Vdd (pin 4) and GND (pin 2) to minimize power supply noise.					

MECHANICAL DRAWING

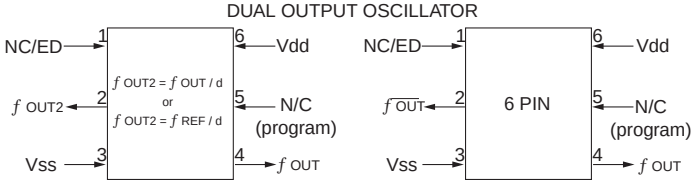


PIN CONFIGURATION

CONVENTIONAL OSCILLATOR



DUAL OUTPUT OSCILLATOR



Pin 2 becomes 2nd Output / Ref. for Dual Freq. or PECL operations.

HEC, INC. HOORAY USA • 30961 WEST AGOURA RD., SUITE 311 • WESTLAKE VILLAGE CA USA 91361
TEL: 818-879-7414 • FAX: 818-879-7417 • EMAIL: sales@hoorayusa.com • INTERNET: www.hoorayusa.com

PECL OUTPUT OPTION

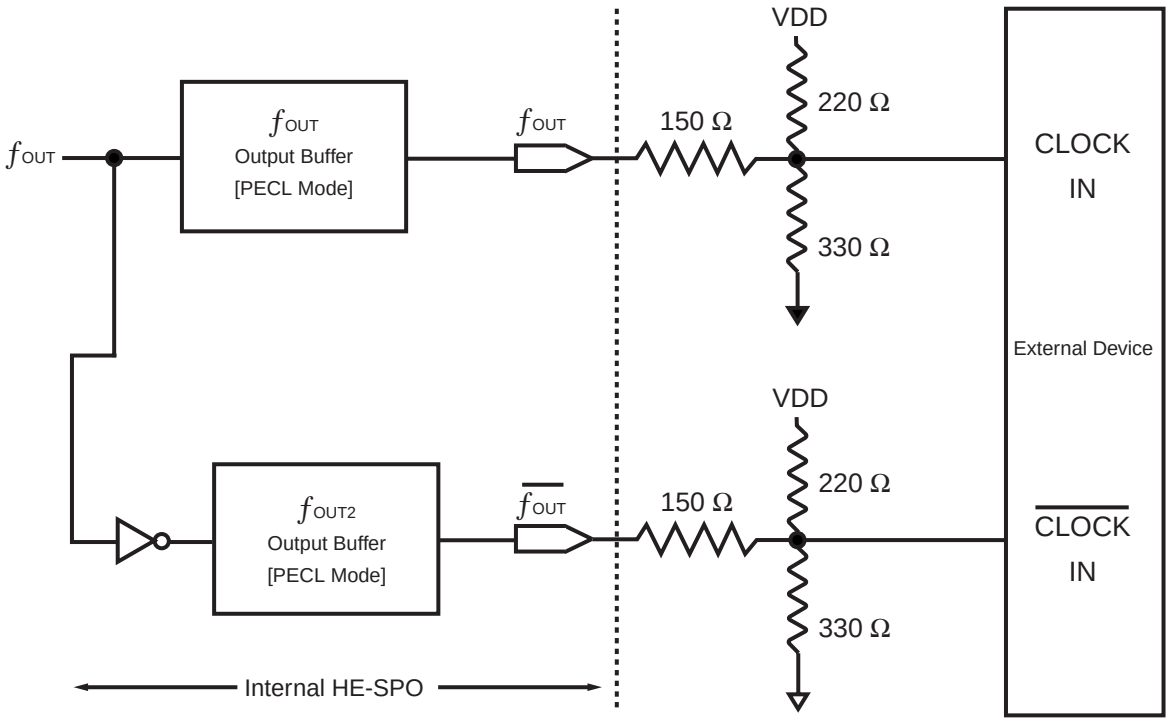
PECL is, simply put, a method of obtaining high-speed low-noise differential outputs from CMOS circuitry. Similar to ECL, PECL utilizes Positive ECL voltage values. This option places the complement of the f_{OUT} signal on the f_{OUT2} output, while maintaining a low skew between the signal edges.

Typically these signals have very low voltage swings (such as 0.6 max.), thus producing very little unwanted radiation which can be generated. The other major advantage is that the complementary pair allows what is called “common mode noise rejection.” In essence, you can filter out all noise which is common on both lines. This interface is quickly becoming the standard for new high-end disk drives (Fiber Channel), new high speed networking (Gigabet Ethernet), and high-end graphics.

The figure below illustrates a typical external interface from the HE-SPO to a device which requires PECL clock.

PECL Interface Example

VDD = 5V



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